IN THE SPECIFICATION

Please replace paragraph [0013] of the specification as originally filed (paragraph [0028] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0013].

[0013] Figure 1 illustrates an apparatus 100 in accordance with an exemplary embodiment of the present invention. The apparatus 100 includes an upper electrode 10, a bottom electrode and stage 20, an edge electrode 30, and insulating plate 40, an RF power supply 50, an isolator and/or insulator 60, a center nozzle 70, and a process nozzle 80. In the apparatus 100 as shown in Figure 1, the upper electrode 10 and the edge electrode 30 are anodes and the bottom electrode 20 is a cathode. However, each of these may be reversed in other exemplary embodiments of the present invention. As shown in Figure 1, the bottom electrode 20 supports the wafer 1 while the upper electrode 10 and the edge electrode 30 reciprocally generate plasma at an edge and/or a backside of the wafer 1. An etching portion A at the edge of the wafer 1 is where the desired etching should take place. Because RF power is supplied from the RF power line 50 through the wafer 1, a lower power generates sufficiently proper plasma to etch thin film layers on the wafer 1. An example of a lower power is 500 W. If the RF power is high, which is generally used in a normal semiconductor etcher, arcs may be caused at the edge bead.

Please replace paragraph [0016] of the specification as originally filed (paragraph [0031] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0016].

[0016] Figure 4A illustrates the bottom electrode and stage 20 of Figure 1 in an exemplary embodiment of the present invention. As shown in Figure 4A, the bottom electrodes 20 includes one or more grooves 31. The one or more ~~groves~~ grooves 31 reduce the likelihood or prevent the wafer 1 from sliding off the bottom electrode and stage 20. As shown in Figure 4A, the one or more grooves 31 are shown as straight lines radiating from the center of the bottom electrode and stage 20. In other exemplary embodiments, the grooves 31 may be curved lines, In ~~the~~ other exemplary embodiments of the present invention, the straight and/or curved grooves 31 may radiate from other than the center of the bottom electrode and stage 20. In exemplary embodiments of the present invention, the grooves 31 form an open pattern, as opposed to a closed pattern, such as a circle, rectangle, triangle, etc. In exemplary embodiments of the present invention, the bottom electrode and stage 20 may include one or more bolt holes 33 and/or one or more lift pin holes 35.

Please replace paragraph [0019] of the specification as originally filed (paragraph [0034] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0019].

[0019] In exemplary embodiments of the present invention, the upper electrode 10 and the insulating plate 40 ~~includes~~ include one or more bolt holes 74c, 79b, respectively, to connect the insulating plate 40 to the upper electrode 10. In other exemplary embodiments of the present invention, the insulating plate 40 includes one or more bolt holes 79a to connect the insulating plate 40 to the one or more supplemental insulating plates 79d.

Please replace paragraph [0020] of the specification as originally filed (paragraph [0035] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0020].

[0020] Figure 4C illustrates a lower portion where the wafer 1 is loaded. As shown in Figure 4C, a first insulator 84 (which may be in the shape of a ring) and a second insulator 85 (which may be in the shape of a cylindrical plate) may be utilized between the bottom electrode and stage 20 and the edge electrode 30.

Please replace paragraph [0025] of the specification as originally filed (paragraph [0040] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0025].

[0025] It is noted that the various exemplary embodiments of the insulating plate illustrated in Figures 2 and [[4]] 3 and/or the various exemplary embodiments of the bottom electrode and stage 20 illustrated in Figures 4 and 5 may also be utilized in the exemplary embodiment illustrated in Figure 6.

Please replace paragraph [0027] of the specification as originally filed (paragraph [0042] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0027].

[0027] It is noted that the various exemplary embodiments of the insulating plate illustrated in

Figures 2 and 3 and the various exemplary embodiments of the bottom electrode and stage 20 illustrated in Figures 4 and 5, may also be utilized in conjunction with the exemplary embodiment illustrated in Figure 7.

Please replace paragraph [0030] of the specification as originally filed (paragraph [0045] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0030].

[0030] The insulating layer 330 may be of a boron-doped phosphosilicate glass (BPSG) or tetraethylorthosilicate (TEOS) of thickness 3000-8000 Å. The tungsten (W) layer 340 may be formed using WF_6 gas and may have a ~~o~~-thickness of 300 to 1000 Å. The first and second nitride layers ~~330,~~ 350 may be of a thickness of 1500-3500 Å and 150-750 Å, respectively, and formed using SiH_4+NH_3 gas. The oxide layer 360 may be formed using SiH_4+O_2 gas and of a thickness of 1000-5000 Å.

Please replace paragraph [0037] of the specification as originally filed (paragraph [0052] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0037].

[0037] Figure 13 illustrates a plot of the gap 44 between the insulating plate 40 and the upper electrode 10 (the x-axis) versus the length L from a center of a wafer to the endpoint of the wafer (the y-axis) in exemplary embodiments of the present invention. As shown in Figure 13, L plus A equals the radius of the wafer 1. For example, the first point in Figure 13 indicates that an

etching portion A of 2.4 mm is produced using a 200 mm diameter wafer (100 mm radius wafer) and a gap 44 increases, L decreases (and correspondingly, A increases).

Please replace paragraph [0040] of the specification as originally filed (paragraph [0055] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0040].

[0040] Figure 15 illustrates a cross-sectional view of a plasma processing apparatus for processing the edge of a wafer in accordance with an exemplary embodiment of the present invention. As shown, the plasma processing apparatus may include a chamber 70, a chamber wall 71, an elastic part 71a, a wafer inlet/outlet 72, a purging gas ~~inlet~~ supply line 73 to supply a purge gas after etching, an upper electrode 10, a support 74a for the upper electrode 10, a stem 74b, a source of process gas 75, a process gas line 75a, a source of inert gas 76, an inert gas line 76b, a plate 77 of the upper electrode 10, which can move up and down, a support 77a for the plate 77 of the upper electrode 10 a driver 78 for the plate 77 of the upper electrode 10, an insulating plate 40, a supplemental insulating plate 40a, a supplemental gas outlet 79c, a wafer 1, a bottom electrode and stage 20, a first insulator 84, a second insulator 85, an edge electrode 30, a lift pin 88 (to receive and load the wafer 1 on the bottom electrode and stage 20), a baffle plate 90 (to exhaust process gas or inert gas uniformly), a sensor 91, a control element 91b, a coolant line 92, operating with a source of coolant 94 to control a temperature of the bottom electrode and stage 20 or the wafer 1, an RF power source 96, a lift pin plate 97, a driver 98 for the left pin plate 97, and an exhaust pump 99. The upper electrode 10 and the insulating plate 40 may be moved between an upper portion and a lower portion by the plate of the upper electrode 77 and

the sensor 91 (for example, a laser sensor) may be located on the chamber wall 71 to detect positions of the upper electrode 10 and the insulating plate 40 on a movement path of the plate of the upper electrode 77. The control element 91b may be located at an upper portion of the chamber wall 71 of the chamber 70 and may control movement of the plate of the upper electrode 77 in response to a signal from the sensor 91.

Please replace paragraph [0041] of the specification as originally filed (paragraph [0056] of U.S. Patent Application Publication No. US 2004/0238488 A1) with the following amended paragraph [0041].

[0041] In an exemplary embodiment, the processing apparatus may include more than one chamber. In an exemplary embodiment, the apparatus includes more than one preparing station, more than one process chamber, ~~and~~ more than ~~the~~ one purging chamber, and at least one transfer chamber. In this manner, one wafer may be loaded, while another wafer is being transferred, and yet another wafer is being processed.